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STATS ChipPAC/PATENT LAW GROUP:
Atkins and Associates, P.C.
55 N. Arizona Place, Suite 104
Chandler, AZ 85225

EXAMINER
CLARK, SHEILA V

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte RAJENDRA D. PENDSE, KYUNGOE KIM, and TAEWOO KANG

Appeal 2016-002169
Application 13/529,794[1]
Technology Center 2800

Before PETER F. KRATZ, WESLEY B. DERRICK, and CHRISTOPHER C. KENNEDY, *Administrative Patent Judges*.

KRATZ, *Administrative Patent Judge*.

DECISION ON APPEAL

This is a decision on an appeal under 35 U.S.C. § 134(a) from the Examiner's decision rejecting claims 20, 22, 26, 28, 32, 34, and 39.[2] We have jurisdiction pursuant to 35 U.S.C. § 6.

We Reverse.

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[1] According to Appellants the Real Party in Interest is STATS ChipPAC, Ltd.

[2] Pending claims 21, 23–25, 27, 29–31, 33, 35–38, and 40–43 stand objected to by the Examiner.

Appellants' claimed invention is directed to a semiconductor device including a substrate having an interconnect site and a bump having a width less than a length at the interconnect site. Further details can be derived from a reading of claims 20 and 32, which claims are illustrative and reproduced below:

> 20. A semiconductor device, comprising:
>
> a substrate including an interconnect site;
>
> a semiconductor die including an interconnect pad, the semiconductor die disposed over the substrate; and
>
> a bump material disposed between the interconnect pad and interconnect site in contact with the interconnect site at a contact surface, wherein a width of the contact surface of the interconnect site in a direction across the interconnect site is less than a length of the contact surface of the interconnect site in a direction along the interconnect site.

> 32. A semiconductor device, comprising:
>
> a substrate including an interconnect site; and
>
> a bump formed over the interconnect site, wherein a width of the bump at the interconnect site in a direction across the interconnect site is less than a length of the bump at the interconnect site in a direction along the interconnect site.

The Examiner maintains the following grounds of rejection:

Claims 20, 22, 26, 28, 32, 34, and 39 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Iwasaki.

We reverse the stated rejection for substantially the reasons argued by Appellants (Reply Br. 1–15; App. Br. 6–16). We add the following for emphasis.

The Examiner bears the initial burden of establishing a prima facie case of anticipation. *In re King*, 801 F.2d 1324, 1326-27 (Fed. Cir. 1986). Anticipation under 35 U.S.C. § 102 requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999).

We agree with Appellants that the Examiner has not carried the burden to establish that the subject matter of the rejected claims is anticipated by Iwasaki. In particular, the Examiner has not reasonably established that Iwasaki describes a contact surface width of an interconnect site in a direction across the interconnect site that is less than a contact surface length of the interconnect site in a direction along the interconnect site as required by independent claim 20.

For instance and with respect to claim 20, the Examiner finds that (Final Act. 2):

> Iwasaki et al teaches in for example figure 12A a semiconductor device, comprising a substrate 11 including an interconnect site 12; and a semiconductor die including an interconnect pad 5 (or 2), the semiconductor die 1 being disposed over the substrate including bump material 13 disposed between the interconnect pad and interconnect site shown in contact with the interconnect site at a contact surface (where 21 meets 12), wherein a width (shown at 21) of the contact surface on the interconnect site in a direction across the interconnect site is shown less than a length of the contact surface of the interconnect site in a direction along the interconnect site, (see also figure 12c).

Contrary to the Examiner's finding and as argued by Appellants (App. Br. 7–8):

> FIG. 12C of Iwasaki shows a cross section of portion 21 of conducting connector 13 having a circular or round shape. Because portion 21 of conducting connector 13 has a round cross-sectional shape, the contact surface between conducting connector 13 and terminal electrode 12 would also be round in shape. The contact surface of conducting connector 13 and terminal electrode 12, therefore, does not have a width of the contact surface in a direction across the interconnect site that is less than a length of the contact surface in a direction along the interconnect site. Rather, the round contact surface on terminal electrode 12 in Iwasaki would have a width (or diameter in a first direction) equal to a length (or diameter in a second direction). Additionally, terminal electrode 12 is not disclosed as having a width less than a length. Because neither conducting connector 13 nor terminal electrode 12 in Iwasaki are disclosed as having a width less than a length, the contact surface between conducting connector 13 and terminal electrode 12 would not produce the claimed shape.

Nor has the Examiner established that Iwasaki describes the corresponding relative bump width and length limitations of independent claims 26, 32, and/or the relative bump interface surface width and length limitation of independent claim 39, as argued by Appellants (App. Br. 9–16).

We concur with Appellants that the Examiner's rebuttal argument is premised on an unreasonable interpretation of Appellants' claims and fails to refute Appellants' argument that the Examiner has not established that Iwasaki anticipates any of the rejected claims (Reply Br. 1–15; Ans. 2–8). Moreover, the Examiner's passing reference to certain other embodiments/figures of Iwasaki in rebuttal (Ans. 7) falls short of

establishing, in the first instance, that Iwasaki provides an anticipating disclosure for any of the rejected claims, as urged by Appellants (Reply Br. 14–15).

It follows that we shall reverse the Examiner's anticipation rejections.

CONCLUSION

The Examiner's decision to reject the appealed claims is reversed.

REVERSED